

Appl. No. 10/708,399  
Amdt. dated March 15, 2006  
Reply to Office action of February 07, 2006

**Amendments to the Drawings:**

Figures 2 and 3 have been amended to replace the incorrectly spelled word "prot" with "port". No other changes have been made, and no new matter has been added. Acceptance of the corrected drawings is respectfully requested.

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Attachment: Replacement Sheets

2 pages

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### REMARKS/ARGUMENTS

#### 1. Rejection of claims 1-8 and 11-13 under 35 U.S.C. 103(a):

Claims 1-8 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Admitted Prior Art (AAPA) in view of Peleg et al (US 6,557,065) further in view of Baxter (US 6,813,689).

#### Response:

The applicant would like to point how the patentable differences between claim 1 and the cited prior art. The claimed invention according to claim 1 claims an expansion port connected to the high-speed bridge circuit. The expansion port connects to an expanding bridge circuit for controlling signal transmission between the high-speed bridge circuit and a low-speed peripheral device.

The AAPA teaches a high-speed bridge circuit 34 and a low-speed bridge circuit 36, but does not teach that an expansion port is connected to the high-speed bridge circuit 34.

Although Peleg teaches a Southbridge 30 connected to the SOC 400, Peleg does not teach that the Southbridge 30 is connected to a high-speed bridge circuit of the SOC 400, as is recited in claim 1. Therefore, neither the AAPA nor Peleg teach an expansion port connected to a high-speed bridge circuit.

Baxter teaches that I/O bridges 37 and 43 are connected to memory 39 through buses 34 and 35 and through ASIC 38. However, Baxter's memory 39 is not analogous to Peleg's Southbridge 30 since the memory 39 is not used to connect additional peripheral devices. Furthermore, although Baxter teaches I/O bridge 37 and I/O bridge 43, Baxter only teaches that peripheral devices 17 are connected to

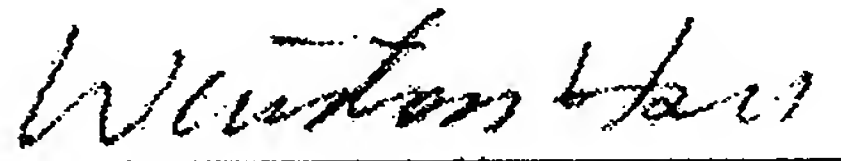
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the I/O bridge 37, but does not teach peripheral devices connected to the I/O bridge 43. Instead, Baxter only teaches requesting processes 10 connected to the I/O bridge 43.

5 For these reasons, it would not be obvious to combine the teachings of Baxter with that of the AAPA and Peleg. Furthermore, since none of the cited prior art clearly teach an expansion port connected to a high-speed bridge circuit, claim 1 is patentably distinguished from the combination of cited prior art references. Claims 2-13 are dependent on claim 1, and should be allowed if claim 1 is allowed.  
10 Reconsideration of claims 1-13 is respectfully requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

15 Sincerely yours,



Date: 03.15.2006

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25 is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)